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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/718,662	11/24/2003	Edwin C. Kan	KAN 2768B	1620

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EXAMINER	
LAM, DAVID	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 04/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/718,662	KAN ET AL.	
	Examiner	Art Unit	
	David Lam	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) *10-12* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Allowable Subject Matter

1. Prosecution on the merits of this application is reopened on claims 1-9 considered unpatentable for the reasons indicated below:

Claim Objections

Claims 1-7 objected to because of the following informalities:

- In claims 1, 3-5, lines 7, 2, 1, 2, respectively, "said nanocrystals" should be change to – said metal nanocrystals --;

- In claim 2, line 1, "said embedded nanocrystals" should be change to – said embedded metal nanocrystals --;

- In claims 6-7 recites the limitation "said first and second storage elements" in line 2 of claims 6, 7. There is insufficient antecedent basis for this limitation in the claims. It appears that should be change to -- first and second storage elements --. Appropriate correction is required.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-2, 4-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eitan (5,768,192) in view of Lee et al. (6,768,165).

Regarding to claims 1 and 8, Eitan discloses a multibit storage cell comprising: a semiconductor substrate (12 or 62) having source (14 or 58) and drain (16 or 60) regions separated by an channel region; a charge storage (trapping) layer on the substrate including an insulation material (18 or 22, 52 or 56); a gate electrode (24 or 50) on the charge storage layer; bias voltage connected to the source and drain regions to produce asymmetric charging of the charge storage; wherein the bias voltages include first and second write voltages connectable to the source and drain to write information to a first storage element, and being reversible to write

information to a second storage element (Cols, 5-6; lines 56-67, 1-10, respectively; Cols. 15-16, lines 41-67, 1-20, respectively). *See at least Figs. 2-3,5, for example, in Col.12 lines 6-12, 55-67; Col. 13, lines 1-10; Col. 14, lines1-67, Col. 20, lines 24-35 and the related disclosure.*

Regarding to claims 2, 4-5; Eitan further discloses wherein the charge storage include a first portion forming a first node (21 or 53) located in the region of a source side junction with the channel and a second portion forming a second node (23 or 55) located in the region of a drain side junction with the channel, the first and second nodes forming first and second storage elements (bits); wherein the gate electrode overlies the charge storage and the channel; wherein the bias voltage are connected to write and read multiple bits of data in the charge storage. *See at least Figs. 2-3,5, for example, in Col.12 lines 6-12, 55-67; Col. 13, lines 1-10; Col. 14, lines1-67, Col. 20, lines 24-35 and the related disclosure.*

With respect to claims 6-7 and 9; Eitan further discloses wherein the bias voltages include write voltages selected to independently write data to the storage elements, and wherein the bias voltages include read voltages selected to independently read data to the storage elements; wherein the bias voltages include first and second read voltages connectable to the source and drain to read information written to the element, and being reversible to read information written to a second storage element (Cols, 5-6; lines 56-67, 1-10, respectively; Cols. 15-16, lines 41-67, 1-20, respectively). *See at least Figs. 2-3,5, for example, in Col.12 lines 6-12, 55-67; Col. 13, lines 1-10; Col. 14, lines1-67, Col. 20, lines 24-35 and the related disclosure.*

Eitan lack an inclusion of wherein the charge storage layer incorporating embedded metal nanocrystals.

Lee et al. disclose a memory device comprising charge storage layer incorporating embedded metal nanocrystals. *See at least Fig. 6, for example, in Col. 18, lines 20-47; Fig. 16, for example, in Col. 22, lines 29-42, and the related disclosure*

It would have been obvious to one having ordinary skill in the art at the time of the invention to provide charge storage layer incorporating embedded metal nanocrystals of Eitan as taught by Lee et al. in order to reduce charge leakage, cost and high-speed access semiconductor memory device.

4. Claim 3 rejected under 35 U.S.C. 103(a) as being unpatentable over Eitan (5,768,192) in and Lee et al. (6,768,165) as applied to claim 1 above, and further in view of Sadd (6,400,610).

Regarding to claim 3, Eitan and Lee disclose all the elements as applied to claim 1 above.

Eitan and Lee lack an inclusion of wherein the insulator material includes a control layer between the gate electrode and the nanocrystals and a tunnel layer between the nanocrystals and the substrate.

Sadd discloses a memory device comprising insulator material includes a control layer (202) between the gate electrode (204) and the nanocrystals (200) and a tunnel layer (102) between the nanocrystals and the substrate (100). *See at least Figs. 4-6, for example, in Cols. 5-6, lines 51-67, 1-39, respectively, and the related disclosure.*

It would have been obvious to one having ordinary skill in the at the time of the invention to provide the insulator material of Eitan and Lee that includes a control layer between the gate

electrode and the nanocrystals and a tunnel layer between the nanocrystals and the substrate, as taught by Sadd in order to reduce charge loss, power supply, and lower access time in semiconductor memory device.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Lam whose telephone number is 571-272-1782. The examiner can normally be reached on 6:00 – 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarabian Amir can be reached on 571-272-1852852. The fax phone numbers for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

D. Lam

April 6, 2006

DAVID LAM
PRIMARY EXAMINER